	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L2	32	1 and interposer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/10/15 13:28
2	BRS	L1	222	chips and coupling and assembly and dicing	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/10/15 13:30
3	BRS	L3	9806	chip with assembl$3	USPAT; US-PGPUB	2001/10/15 13:44
4	BRS	L4	340	3 and interposer	USPAT; US-PGPUB	2001/10/15 13:44
5	BRS	L5	313	4 not 1	USPAT; US-PGPUB	2001/10/15 13:44
6	BRS	L6	174	5 and testing	USPAT; US-PGPUB	2001/10/15 13:44
7	BRS	L7	27	6 and dicing	USPAT; US-PGPUB	2001/10/15 13:45
8	BRS	L8	213	(matched adj set) and chip and assembly	USPAT	2001/10/15 14:07
9	BRS	L9	0	8 and testing and dicing	USPAT	2001/10/15 14:08
10	BRS	L10	190	8 and testing	USPAT	2001/10/15 14:10
11	BRS	L14	14	438/14.ccls. and assembl$3 and testing and dicing	USPAT	2001/10/15 14:19
12	BRS	L15	18	438/15.ccls. and assembl$3 and testing and dicing	USPAT	2001/10/15 14:24

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	Type	L #	Hits	Search Text	DBs	Time Stamp
13	BRS	L16	0	438/480.ccls. and assembl$3 and testing and dicing	USPAT	2001/10/15 14:25
14	BRS	L17	14	257/48.ccls. and assembl$3 and testing and dicing	USPAT	2001/10/15 14:25

	Type	Hits	Search Text
1	BRS	19	(wafer with interposer with assembly) and @ad<=20001002
2	BRS	1	(wafer with interposer with assembly) and @ad<=20001002
3	BRS	7	wafer and chips and dicing and (matched with set)

	DBs	Time Stamp
1	USPAT; US-PGPUB	2001/10/15 13:10
2	EPO; JPO; DERWENT; IBM TDB	2001/10/15 13:11
3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/10/15 13:12

DOCUMENT-IDENTIFIER: US 5563086 A
TITLE: Integrated memory cube, structure and fabrication

BSPR:
Conventionally, integrated circuit devices, such as memory devices, have been made from wafers of semiconductor material which include a plurality of integrated circuits. After a wafer is made, the circuits are separated from each other by **dicing** the wafer into small chips. Thereafter, the chips are bonded to carriers of various types, electrically interconnected by wires to leads and packaged.

BSPR:
Traditionally, computer memory systems are **assembled** from many types of memory chips, such as, DRAMs, SRAMs, EPROMs and EEPROMs. The number of storage devices per memory chip technology generation varies but increases over time with more devices per chip being delivered with each succeeding generation, thereby providing greater memory capacity. When a next generation memory chip becomes available, the number of chips needed to make a given memory system is correspondingly reduced. With fewer memory chips needed, the resultant memory system becomes physically smaller.

BSPR:
A number of advantages are inherent in an integrated memory cube structure and fabrication approach in accordance with the invention. For example, the resultant structure can emulate a next generation memory chip using readily available existing generation memory chips. The cube can have physical dimensions within industry standards for a next generation memory chip.
Testing and burn-in of the logic chip and memory chips can be separately conducted. Further, any number of semiconductor chips can be

employed within
the cube. The number employed depends upon the memory chip architecture
selected and the memory cube architecture desired.

DEPR:
An integrated memory cube in accordance with the invention can be implemented
using any one of a variety of available memory chip architectures. By way of
example, the following discussion assumes that four 16 Mb DRAMs are to be
assembled in a stack. This memory cube emulates exactly a next generation
memory chip, i.e., a 64 Mb DRAM. This integrated function is accomplished by
associating a control logic chip with the stack of four memory chips. The
resultant cube of four 16 Mb DRAMs plus logic chip can be sized to fit within
an industry standard 64 Mb package, or if desired, a smaller package. Compared
with single memory chips, there are significant processing, manufacturability
and cost advantages to an integrated memory cube structure in accordance with
this invention.

DEPR:
Further, very little semiconductor area is required to implement the logic
functions described below. Therefore, extra area within logic chip 14' can be
used for customer-specific applications. These applications include SRAM,
psuedostatic RAM, error correction code, memory handshaking, and array built-in
self-**testing**. Inclusion of such applications on logic chip 14' could
dramatically improve performance of the cube for
customer-specific uses.

DEPR:
Referring to FIG. 5, a preferred processing approach is to produce multiple
subassemblies 110 comprising stacked memory chips 114, logic chip 114' and a
preformed spacer layer 118, for example, fabricated of Upilex. As shown in
FIG. 6, these memory subassemblies are produced by stacking and

laminating the
individual components (114, 114'and 118) in the preferred
configuration.
Segmentation layer 112 (e.g., parylene), interposed between
memory
subassemblies 110, is incorporated into stack 120 to facilitate
segmentation of
the subassemblies. Side face processing is comprised of
insulation layer 115
and metallization layer 116. Once side surface metallization is
complete, the
subassemblies are segmented and cleaned. The resulting **assembly**
of logic chip,
memory chips and Upilex comprises the functional portion of the
cube. Once the
lead frame is connected, the **assembly** can then be packaged using
standard
plastic encapsulation technology currently used for single-chip
memory chips.

DEPR:
Thus, cube fabrication is subdivided into five basic process
sectors: (1)
wafer-level processing where the transfer metal, polyimide
passivation, and
Thermid.RTM. polymer (trademark of National Starch and Chemical
Co.) are
deposited/applied onto the memory and logic chips still in wafer
form; (2) dice
and lamination processing where the wafers are diced into
individual chips,
then stacked and laminated into a cube format (FIG. 5) with upper
layers of
Upilex 118 and parylene segmentation polymer 112 (FIG. 6); (3)
cube-level
processing where thin-film deposition occurs on an **assembly** side
surface (This
last sector results in the electrical interconnection of the
individual memory
chips and the logic chip, and fabrication of a functional
integrated memory
cube.); (4) attachment and interconnection of the cube and lead
frame; and (5)
plastic encapsulation of this **assembly**.

DEPR:
The basic approach to segmentation is one where the temperature
of the extended
stack is elevated to a point for which a phase transition in the
segmentation

material occurs and a shear force is applied to the stack **assemblies**. Another approach would be one for which the temperature of the cubes is lowered to a point where the mechanical properties of the segmentation material are altered such that facile segmentation is possible. One can envision the limit of this being a cryogenic separation process where the temperature is lowered to a point that the segmentation material becomes extremely brittle and the extended stack literally falls apart into the constituent cubes.

DEPR:
At this point, **assembly** of the logic chip, spacer layer, and memory chips is completed. The resultant structure is a stand alone microelectronic entity that emulates a single integrated circuit memory chip. The last step in the fabrication process is to "package" this entity. The most common way to package memory chips is to interconnect the chip I/O to a lead frame and then encapsulate the lead frame/chip **assembly** using plastic, i.e., to form a TSOP or SOJ. The same is done for an **assembled** structure in accordance with the present invention. Industry standard practices and materials for lead frame attachment, wirebond interconnection, and plastic encapsulation, using injection molding techniques, can be used to package this **assembly**. Once encapsulated, fabrication and packaging of the integrated memory module cube is complete.

DEPR:
As set forth above, there are a number of inherent advantages in the integrated memory cube structure and fabrication approach of the present invention. The resultant structure emulates a next generation memory chip using readily available existing generation memory chips. Further, a cube can have physical dimensions within industry standards for an initial next generation memory

chip. **Testing** and burn-in of the logic chip and memory chips can be separately conducted, thereby identifying a potential defect at a lower level of **assembly**. Further, any number of semiconductor chips can be employed within a cube. The number employed depends upon the memory chip architecture selected and the memory cube architecture desired.

DEPV:
1. a sufficient adhesive strength to "hold" stack **assemblies** together for side surface processing;

DEPV:
4. segmentability, i.e., allows segmentation of stacked cube **assemblies** at a temperature below approximately 400.degree. C. (essentially it must be a material that goes through an appropriate phase transition below 400.degree. C.); and

DEPV:
2. Laminate this **assembled** structure using elevated pressure and temperature;

DEPW:
b. Separate cube **assembly** from cube stack

DEPX:
Each cube **assembly** in the large stack it treated independently from a photolithographic standpoint; therefore, cube **assembly** stacking tolerances are not critical;

CLPR:
10. The fabricating method of claim 1, further comprising the step of **testing** and burning-in each of the N memory chips and the logic chip prior to said stack forming step (c).

CCOR:
438/15

DOCUMENT-IDENTIFIER: **US 6288559 B1**
TITLE: Semiconductor testing using electrically conductive adhesives

DID:
US 6288559 B1

APD:
19980330

BSPR:
A third embodiment of the method of the present invention includes the steps of (1) flowing C4s onto **wafer** pads; (2) positioning a non-conductive **interposer** between the **wafer** and the substrate so that vias in the **interposer** are aligned with the contacts on the **wafer** and substrate, the vias being filled with ECA material; (3) moving the **wafer** and the substrate together and applying a predetermined force so that the ECA material conforms to the C4 bumps and pads of the substrate; (4) testing the **wafer**; and (5) removing the **interposer**, thereby readying the C4s for attachment into a final **assembly**.

DOCUMENT-IDENTIFIER: **US 6281046 B1**
TITLE: Method of forming an integrated circuit package at a wafer level

DID:
US 6281046 B1

APD:
20000425

ABPL:
A method of forming an integrated circuit package at the wafer level. The integrated circuit package occupies a minimum amount of space on an end-use printed circuit board. Solder bumps, or conductive adhesive, is deposited on the metallized wirebond pads on the top surface of a silicon wafer. An underfill-flux material is deposited over the wafer and the solder bumps. A pre-fabricated interposer substrate, made of metal circuitry and a dielectric base, has a plurality of metallized through-holes which are aligned with the solder bumps. The wafer/interposer **assembly** is reflowed, or cured, to form the electrical connection between the circuitry on the **interposer** layer and the circuitry on the **wafer**. Solder balls are then placed on the metal pad openings on the interposer substrate and are reflowed to form a wafer-level BGA structure. The wafer-level BGA structure is then cut into individual BGA chip packages.

BSPR:
The above objects have been achieved in a method of forming an integrated circuit package on the wafer level using a flip chip design with a single wafer. The integrated circuit package is formed by first providing a product silicon wafer having a plurality of microelectric circuits fabricated thereon and having a plurality of standard aluminum bonding pads exposed.

The aluminum
bonding pads are re-metallized to be solderable. Then, a plurality of solder
bumps are deposited on the bonding pad sites. Then, a layer of underfill-flux
material is deposited onto the wafer surface, over the solder bumps. A
pre-fabricated **interposer** substrate, having metallized through-holes, is
aligned to the **wafer and then the assembly** is reflowed, or cured, to secure the
interposer substrate to the layer of underfill-flux material, and to form the
electrical connection between the circuitry on the substrate and the bonding
pads on the silicon **wafer**. Solder balls are then placed on the metal pad
openings on the interposer substrate and are then reflowed forming a BGA
structure. The wafer is then diced and the individual BGA packages are formed.
The BGA package is ready for the next level assembly.

DEPR:
With reference to FIG. 6, the **interposer** substrate 31 is then adhered to the
wafer 21 by the underfill-flux material 27 and the wafer/interposer **assembly** 39
is then cured. Thus, the interposer is aligned and bonded to the wafer.

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1 **Fab Integrated Packaging (FIP): a new concept for high reliability wafer-level chip size packaging**
Topper, M.; Auersperg, J.; Glaw, V.; Kaskoun, K.; Prack, E.; Keser, B.; Cosk Jager, D.; Fetter, D.; Ehrmann, O.; Samulewicz, K.; Meinherz, C.; Fehlberg, Karduck, C.; Reichl, H.
Electronic Components & Technology Conference, 2000. 2000 Proceedings. 2000
Page(s): 74 -80

[Abstract] [PDF Full-Text (624 KB)] **CNF**

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2 **Over-coated flip-chip fine package development for MCM fabricate IC and GaAs MMIC**
Kurata, H.; Ogata, T.; Mitsuka, K.; Matsushita, H.
Electronic Components & Technology Conference, 2000. 2000 Proceedings. 2000
Page(s): 949 -954

[Abstract] [PDF Full-Text (816 KB)] **CNF**

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3 **Wafer level package using double balls**
Topper, M.; Glaw, V.; Coskina, P.; Auersperg, J.; Samulewicz, K.; Lange, M. C.; Fehlberg, S.; Ehrmann, O.; Reichl, H.
Advanced Packaging Materials: Processes, Properties andInterfaces, 2000. Proceedings. International Symposium on , 2000
Page(s): 198 -200

[Abstract] [PDF Full-Text (256 KB)] **CNF**

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4 **Flip-chip fine package and its assembly line devel pment f r GaAs**
Kurata, H.; Ogata, T.; Mitsuka, K.; Matsushita, H.; Kimura, C.
Electronics Manufacturing Technology Symposium, 1999. Twenty-Fourth IEE

1999
Page(s): 214 -221

[Abstract] [PDF Full-Text (1,048 KB)] **CNF**

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5 **Super CSP/sup TM/: WLCSP solution for memory and system LSI**
Hamano, T.; Kawahara, T.; Kasai, J.-I.
Advanced Packaging Materials: Processes, Properties and Interfaces, 1999. Proceedings. International Symposium on , 1999
Page(s): 221 -225

[Abstract] [PDF Full-Text (456 KB)] **CNF**

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6 **Laminated memory: a new 3-dimensional packaging technology fo**
Tuckerman, D.B.; Bauer, L.-O.; Brathwaite, N.E.; Demmin, J.; Flatow, K.; h
Kim, P.; Lin, C.-M.; Lin, K.; Nguyen, S.; Thipphavong, V.
Multi-Chip Module Conference, 1994. MCMC-94, Proceedings., 1994 IEEE , 1
Page(s): 58 -63

[Abstract] [PDF Full-Text (588 KB)] **CNF**

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Super CSP™: WLCSP Solution for Memory and System LSI

Toshio HAMANO
Fujitsu Microelectronics, Inc.
Advanced Packaging Technology
Phone 408-922-9532
Fax 408-954-9462
E-mail thamano@fmi.fujitsu.com

Toshimi KAWAHARA
Fujitsu Ltd.
LSI Packaging Technology Development
Phone +81-44-754-2502
Fax +81-44-754-2334
E-mail kawahara@pkga.ed.fujitsu.co.jp

Jun-ichi KASAI
Fujitsu Ltd.
LSI Packaging Technology Development
Phone +81-44-754-2502
Fax +81-44-754-2334
E-mail kasai@pkga.ed.fujitsu.co.jp

Extended Abstract

Introduction

Wafer Level CSP (WLCSP) has been paid great attention /1/ , because of its ultimate miniature size. It is a Real Chip Size Package from package perspective. It is also a Known Good Encapsulated Die (KGED) from die perspective. It means that the boundary between package and bare die becomes indistinct. It sometimes refers as a 'packageless' package. It is no longer meaningless inquiring which you should chose whether CSP or bare die since WLCSP is coming out. WLCSP is shaped by Wafer Level Packaging (WLP) and Wafer Level Testing (WLT). At this time, eight WLCSPs are proposed using different kind of WLP. Three WLT are also proposed including our technology.

We developed Super CSP™ using unique WLP /2, 3, 4/. It has five major process; re-routing, metal-post forming, compression moulding, ball placing, and dicing. This package allows a system designer to layout a motherboard at the smallest area. It also allows an assembly engineer to mount on a motherboard and replace from the motherboard as conventional CSPs, and allows a test engineer to test and burn-in much easier than Known Good Die (KGD).

We confirmed excellent electrical performance, package reliability, mountability, and second level packaging reliability. This is a report of our findings.

Package design rule

Figure 1 shows the picture of Super CSP™. The package has ball-count of 48. Its ball pitch is 0.75 mm, the body size is 6.8 mm × 6.9 mm, and the height is 1.0 mm in the maximum. Figure 2 shows cross-sectional view and layer structure of this package. The line and space of the redistribution layer of this package are 75 μ m of line and 75 μ m of space. The design rule is summarized in Table 1. One of the disadvantages of WLCSP is that it is impossible to be fan-out configuration. That means it is inevitable to shrink ball pitch based on 20 % reduction rule. We confirmed that it is practicable to be 400 ball-count by 0.40 mm in ball pitch.

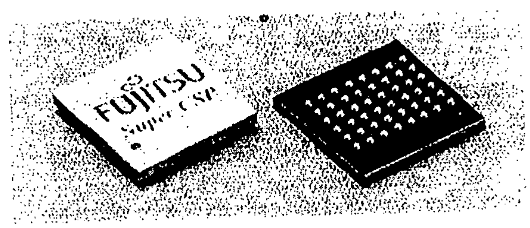


Figure 1. SuperCSP ™ 48 of 0.75mm ball pitch.

Package Process Flow

Super CSP™ is shaped by WLP. Whole process is going through wafer level until ball attachment process illustrated in Figure 3. The process consists of the following: 1) redistribution layer, 2) metal post, 3) compression mould, 4) ball placing, and 5) singulation by dicing. The process begins with spin-coating polyimide dielectric on a die. Adhesion metal is sputtered on the polyimide. Copper is sputtering, and then plating to form a conductive layer of 5 μ m in thickness in the minimum. A redistribution layer is formed by photolithography method in order to redistribute a peripheral pad to an area array terminal. The copper post on the redistribution layer is formed by high speed copper electrolytic plating using a dry film resist (Figure 4). The copper post is unique, because it reduces second level packaging stress. This post is flexible, and its height is 100 μ m. Figure 5 shows the cross-section picture of copper post. Equipment for steppering, spin-coating, sputtering, etching, and plating are

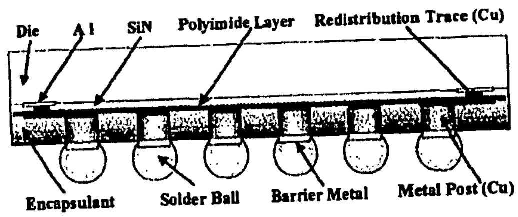


Figure 2. Cross-sectional view and layer structure.

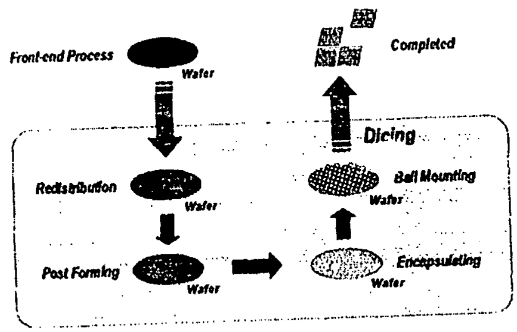


Figure 3. Process flow overview by Wafer Level Packaging.

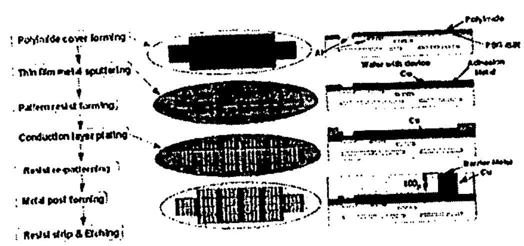


Figure 4. Redistribution and metal post formation.

Figure 5. Copper post.

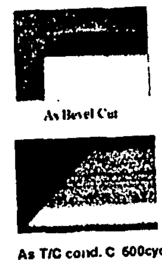


Figure7. Bevel cutting method.

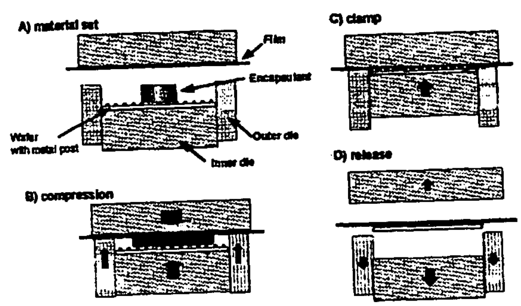


Figure 6. Compression mould method.

converted into the WLP process from secondhand equipment of a front-end process. An encapsulation is implemented by the compression mould method (Figure 6). It is unique with using a temporary film between the die and the upper mould in order to prevent damage to the copper post, and enable the release of the wafer from the mould without resin residue. It enables to use the mould resin of mould-re-leasing agent free, which improve especially adhesion to the die. It also enables to add large amount of the filler in the resin in order to reduce the coefficient of thermal expansion (CTE) to be similar as a printed circuit board. The thick mould resin is also effective against an alpha ray error. The barrier metal, which prevents solder diffusion into the copper post, and the wetting metal for ball attachment are plated onto the copper post. After ball placing, the wafer is singulated to a package. We use Bevel cutting method in order to prevent chipping and delaminating (Figure 7). Both six and eight inch

Table 1. Design rule of 0.80, 0.50, and 0.40 mm in ball pitch

Pin Pitch (Viapost Diameter)	Rows	Chip Size (mm sq.)					Line/Space (μm/μm)
		3.0mm	5.0mm	7.0mm	9.0mm	11.0mm	
0.80 mm (0.35 mm)	5		25	49	100	180	50/40
	6		↑	↑	↑	192	35/35
0.50 mm (0.23 mm)	4	16	64	128	192	256	25/25
	5	↑	↑	140	220	300	20/20
0.40 mm (0.19 mm)	2	25	64	104	144	184	70/70
	3	↑	84	144	204	264	35/35
	4	↑	96	176	256	336	25/25
	5	↑	100	200	300	400	14/14

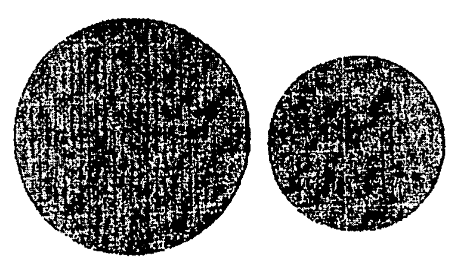


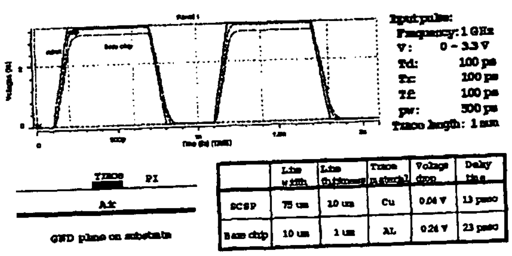
Figure 8. As moulding of 6 (right) and 8 (left) inch wafer.

wafer can be used in this process (Figure 8). Despite the various size of Super CSP™, it can be shaped by using a single mould in each wafer size.

Results and discussion

Electrical performance

The alternative to WLCSP is a KGD. Benefits of WLCSP are easiness to handle in a customer besides cost-effectiveness : 1) area array configuration with coarse ball pitch, 2) no underfill, 3) no clean room facility, 4) existing infrastructure of testing and mounting. Electrical performance of Super CSP™ is, moreover, superior to KGD, because copper trace is routed from peripheral pad area to area-array terminal. Figure 9 shows the result of HSPICE simulation. Voltage drop of Super CSP™ was only – 38 dB as against – 23 dB that of KGD. The delay time of Super CSP™ was only 13 psec as against 23 psec that of KGD. Excellent electrical performance of this package is because of its small resistance of copper trace. The sheet resistance was 4 m Ω .



	Line width	Line thickness	Trace material	Voltage drop	Delay time
SCSP	75 um	10 um	Cu	0.04 V	13 psec
Bare chip	10 um	1 um	AL	0.24 V	23 psec

Figure 9. Results of HSPICE simulation.

Package reliability

WLCSP slims down to the minimum function of a package, which means that it becomes more sensitive to a reliability test. We investigated various reliability tests, such as temperature cycle test, pressure cooker test, high temperature storage test, and moisture sensitivity test. Table 2 shows those results. All data were sufficiently good, and tests are continued. Excellent reliability of Super CSP™ is due to excellent adhesion of the mould resin to the die, in spite of its thin thickness of 100 μ m compared to the conventional CSP.

Table 2. Results of package reliability.

Test	Test Condition		Results
Temperature Cycle	-65/+150°C (Condition-C)	N=10	500cyc. PASS
Pressure Cooker	+121°C/85%RH	N=10	168Hrs PASS
High Temp. Storage	+150°C/ in the air	N=10	500Hrs PASS
Moisture Sensitivity	JEDEC Level 3	N=10	PASS

* Pre-Condition: PB(+125°C/24Hrs) – +85°C/85%RH/24Hrs – IR Reflow(+240°C up)

Mountability

One of the important functions of a package is feasibility of mounting onto a motherboard by using existing equipment. The disadvantage of KGD is that it is necessary to use a special bonding machine to mount onto a motherboard. Super CSP™ has JEDEC standard ball pitch to allow you to use a common mounting machine. Table 3 summarizes the results. Both tray and emboss tape (Figure 10) was used for this test. We confirmed that the mountability of this package was excellent.

Table 3. Results of mounting to a motherboard.

Material	
Package	*Super CSP*™ 45 (p=0.75, ball=ϕ0.35) (Packing; Emboss-tape, Tray)
Solder	KME MSP130-69
Board	FR-4 (Land=ϕ0.35)
Mask	t=0.15, ϕ=0.35
Equipment	
Mounter	KME CM100-M
Printer	KME SP22P-M
Reflow	KME RF10A-MA

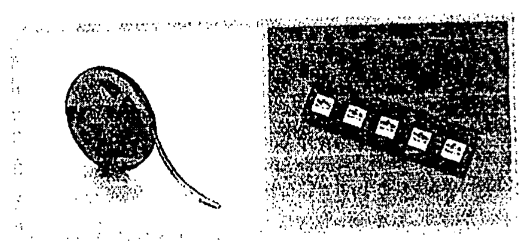


Figure 10. Emboss tape.

Second level packaging reliability

Second level packaging reliability becomes very important, because a WLCSP is influenced by mechanical and thermal stress after mounting on a motherboard. Figure 11 shows the

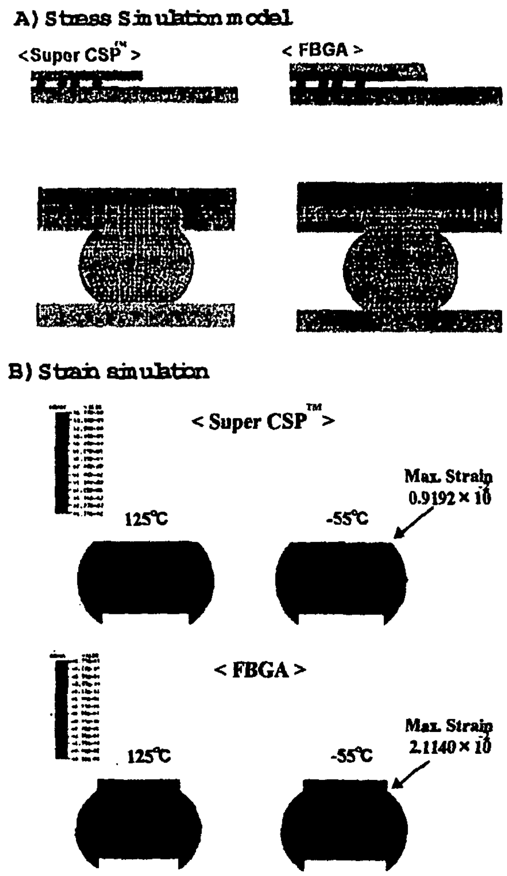


Figure 11. Results of simulated stress analysis.

Table 4. Results of falling test, shear strength, and bending test

Test	Test Condition		Results
Free Fall Test	Vertical / Horizontal 1.5m/150g	N=10	10 Times
Package Shear Test	Shear Speed 0.3mm/sec.	N=10	20.6 Kgf
Bending Test	Bending Span=100mm Bending Speed=5mm/min.	N=10	Over 15mm

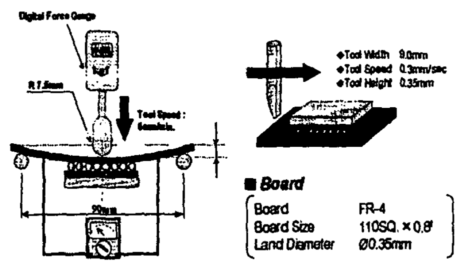


Table 5. Results of temperature cycle and pressur test

Test	Test Condition		Results
Temperature Cycle	-55/+125℃ (Condition-B)	N=10	800cyc. PASS (To be continued)
Pressure Cooker	+121℃/85%RH	N=10	168Hrs PASS

simulated stress analysis result after temperature cycle test. Maximum strain of Super CSP™ at − 55℃ was 0.9 % as against 2.1 % that of FBGA. It indicates that Super CSP™ is advantageous to the stress because of its small size of the package, stress relief by copper post, and the adjustment of CTE of the resin to the motherboard. We investigated various reliability tests. Table 4 shows the results of falling test, shear strength measurement, and bending test data. Table 5 shows the results of temperature cycle test, and pressure cooker test. All data were sufficiently good, and temperature cycle test and pressure cooker test are continued.

Conclusions

Super CSP™ is one of a WLCSP. This package is shaped by unique WLP. We confirmed excellent electrical performance, package reliability, mountability, and second level packaging reliability. Its process TAT is sufficiently short, and it is cost effective because of a consistent WLP. It fits completely accomodating memory including high-speed memory and system LSI devices. We also keep developing WLT technology for a functional test and a burn-in test. Combining WLP and WLT will make Super CSP™ far most suitable for ultimate miniature package.

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